



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Farnworth et al.

Serial No.: 09/589,841

Filed: June 8, 2000

For: STEREOGRAPHIC
METHODS FOR FORMING A
PROTECTIVE LAYER ON A
SEMICONDUCTOR DEVICE SUBSTRATE
AND SUBSTRATES INCLUDING
PROTECTIVE LAYERS SO FORMED

Confirmation No.: 1415

Examiner: G. Lee

Group Art Unit: 2825

Attorney Docket No.: 2269-3923US
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In accordance with 37 C.F.R. § 1.97(g) and (h), filing of this Supplemental Information Disclosure Statement is not to be construed as a representation that a search has been made or an admission that the information cited herein is, or is considered to be, material to patentability as defined in 37 C.F.R. § 1.56(b). Further, no representation is made by Applicants herein that no other possible material information as defined in 37 C.F.R. § 1.56 (b) exists.

U.S. Patent Documents

<u>U.S. Patent No.</u>	<u>Publication Date</u>	<u>Patentee</u>
6,251,488	06/26/01	Miller et al.
6,259,962	07/10/01	Gothait
6,268,584	07/31/01	Keicher et al.
6,326,698	12/04/01	Akram
6,391,251	05/21/02	Keicher et al.
6,432,752	08/13/02	Farnworth
6,482,576	11/19/02	Farnworth et al.
6,489,007	12/03/02	Grigg et al.
6,514,798	02/04/03	Farnworth
6,544,821	04/08/03	Akram
6,544,902	04/08/03	Farnworth
6,549,821	04/15/03	Farnworth et al.
6,562,278	05/13/03	Farnworth et al.
6,585,927	07/01/03	Grigg et al.
6,593,171	07/15/03	Farnworth
6,635,333	10/21/03	Grigg et al.

Other Documents

U.S. Patent Application Publication 2002/0066966 A1 to Farnworth, dated June 6, 2002

U.S. Patent Application Publication 2002/0098623 A1 to Akram, dated July 25, 2002

U.S. Patent Application Publication 2002/0171177 A1 to Kritchman et al., dated November 21, 2002

U.S. Patent Application Publication 2002/0182782 A1 to Farnworth, dated December 5, 2002

U.S. Patent Application Publication 2003/0003180 A1 to Farnworth et al., dated January 2, 2003

U.S. Patent Application Publication 2003/0003380 A1 to Farnworth et al., dated January 2, 2003

U.S. Patent Application Publication 2003/0003405 A1 to Farnworth et al., dated January 2, 2003

U.S. Patent Application Publication 2003/0043360 A1 to Farnworth, dated March 6, 2003

U.S. Patent Application Publication 2003/0068584 A1 to Farnworth et al., dated April 10, 2003

U.S. Patent Application Publication 2003/0072926 A1 to Grigg et al., dated April 17, 2003

U.S. Patent Application Publication 2003/0077418 A1 to Grigg et al., dated April 24, 2003

U.S. Patent Application Publication 2003/0089999 A1 to Akram, dated May 15, 2003

U.S. Patent Application Publication 2003/0092220 A1 to Akram, dated May 15, 2003

U.S. Patent Application Publication 2003/0093173 A1 to Farnworth et al., dated May 15, 2003

U.S. Patent Application Publication 2003/0102566 A1 to Farnworth, dated June 5, 2003

U.S. Patent Application Publication 2003/0129787 A1 to Farnworth, dated July 10, 2003

U.S. Patent Application Publication 2003/0151167 A1 to Kritchman et al., dated August 14, 2003

U.S. Patent Application Publication 2003/0203158 A1 to Farnworth et al., dated October 30, 2003

MILLER et al., "Maskless Mesoscale Materials Deposition" , Deposition Technology, September 2001, pages 20-22

MILLER, "New Laser-Directed Deposition Technology", Microelectronic Fabrication, August 2001, page 16

Webpage, Objet Prototyping the Future, "Objet FullCure700 Series", 1 page

Wepage, Objet Prototyping the Future, "How it Works", 2 pages

U.S. Patent Application No. 09/651,930, filed August 31, 2000, entitled "Semiconductor Device Including Leads in Communication with Contact Pads Thereof and a Stereolithographically Fabricated Package Substantially Encapsulating the Leads and Methods for Fabricating the Same", inventor Salman Akram

U.S. Patent Application No. 10/370,755, filed February 20, 2003, entitled "Chip Scale Package Structures and Method of Forming Conductive Bumps Thereon", inventor Warren M. Farnworth

U.S. Patent Application No. 10/455,091, filed June 5, 2003, entitled "Methods for Stereolithographic Processing of Components and Assemblies", inventor Warren M. Farnworth

U.S. Patent Application No. 10/608,749, filed June 26, 2003, entitled "Methods for Labeling Semiconductor Device Components", inventor Grigg et al.

U.S. Patent Application No. 10/619,918, filed July 15, 2003, entitled "Stereolithographic Methods for Fabricating Hermetic Semiconductor Device Packages and Semiconductor Devices Including Stereolithographically Fabricated Hermetic Packages", inventor Warren M. Farnworth

U.S. Patent Application No. 10/672,098, filed September 26, 2003, entitled "Apparatus and Methods for Use in Stereolithographic Processing of Components and Assemblies", inventor Warren M. Farnworth


U.S. Patent Application No. 10/690,417, filed October 20, 2003, entitled "Methods of Coating and Singulating Wafers and Chip-Scale Packages Formed Therefrom", inventor Farnworth et al.

Applicants offer to supply any explanation or discussion of the documents which the Examiner feels is necessary or desirable and which is requested.

Serial No. 09/589,841

This Supplemental Information Disclosure Statement is believed to be filed before the mailing date of the first Office Action on the merits subsequent to the filing of an RCE in the above-identified application.

Respectfully submitted,

A handwritten signature in black ink, appearing to read "Brick G. Power", with a stylized flourish at the end.

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Date: November 21, 2003
BGP/sls:djp

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PTO/SB/08A (10-01)



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STATEMENT BY APPLICANT**

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Complete if Known

Application Number	09/589,841
Filing Date	June 8, 2000
First Named Inventor	Farnworth et al.
Group Art Unit	2825
Examiner Name	G. Lee
Attorney Docket Number	39231US (99-0033.00/11S)

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
		U.S. Patent Application Publication 2002/0066966 A1 to Farnworth, dated June 6, 2002	
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		Webpage, Objet Prototyping the Future, "Objet FullCure700 Series", 1 page	
		Wepage, Objet Prototyping the Future, "How it Works", 2 pages	
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